

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-162 (canceled)

163. (currently amended) A chip package comprising:

a first insulating layer;

a die between a first portion of said first insulating layer and a second portion of said first insulating layer, wherein said die has a top surface substantially coplanar with a top surface of ~~said first portion of said first insulating layer; and with a top surface of said second portion of said first insulating layer;~~

a second insulating layer on said top surface of said die and ~~[[on]]~~ said top surface ~~surfaces of said first and second portions of said first insulating layer;~~

a ~~[[first]]~~ patterned metal layer over said second insulating layer, ~~[[over]]~~ said top surface of said die and ~~[[over]]~~ said top surface ~~surfaces of said first and second portions of said first insulating layer, wherein said [[first]] patterned metal layer is connected to said die through an opening in said second insulating layer; wherein said first patterned metal layer comprises electroplated copper;~~

a comb-shaped capacitor ~~passive device~~ over said second insulating layer; ~~and, wherein said passive device comprises a passive device portion directly over said top surface of said first portion of said first insulating layer;~~

a third insulating layer on said ~~first~~ patterned metal layer~~[[, on]]~~ and said comb-shaped capacitor, ~~passive device, and~~ over said second insulating layer, ~~[[over]]~~ said top surface of said die and ~~[[over]]~~ said top surface ~~surfaces of said first and second portions of said first insulating layer. [[; and]]~~

~~a metal bump directly over said top surface of said first portion of said first insulating layer, wherein said metal bump is connected to said die through said first patterned metal layer.~~

164. (currently amended) The chip package in claim 163, wherein said comb-shaped capacitor comprises a portion vertically over said first portion of said first insulating layer. ~~passive device comprises a resistor.~~

165. (previously presented) The chip package in claim 163, wherein said passive device comprises a capacitor.

166. (previously presented) The chip package in claim 163, wherein said second insulating layer comprises polyimide.

167. (previously presented) The chip package in claim 163, wherein said second insulating layer comprises benzocyclobutene (BCB).

168. (currently amended) The chip package in claim 163, wherein said patterned metal layer comprises electroplated copper. ~~further comprising a second patterned metal layer on said third insulating layer, over said top surface of said die and over said top surfaces of said first and second portions of said first insulating layer, wherein said second patterned metal layer comprises electroplated copper, wherein said second patterned metal layer is connected to said first patterned metal layer through an opening in said third insulating layer, and wherein said metal bump is connected to said first patterned metal layer through said second patterned metal layer.~~

169. (previously presented) The chip package in claim 163, wherein said third insulating layer comprises polyimide.

170. (previously presented) The chip package in claim 163, wherein said third insulating layer comprises benzocyclobutene (BCB).

171. (currently amended) The chip package in claim 163 further comprising multiple solder bumps configured for external connection. ~~, wherein said metal bump comprises a solder.~~

172. (canceled)

173. (currently amended) The chip package in claim 163 further comprising multiple gold bumps configured for external connection, ~~wherein said metal bump comprises gold.~~

174. (canceled)

175. (canceled)

176. (previously presented) The chip package in claim 163 further comprising a substrate under said die and under said first and second portions of said first insulating layer.

177. (previously presented) The chip package in claim 176, wherein said substrate comprises silicon.

178. (previously presented) The chip package in claim 163, wherein said first insulating layer comprises an epoxy.

179. (currently amended) A chip package comprising:

a first insulating layer;

a die between a first portion of said first insulating layer and a second portion of said first insulating layer, wherein said die has a top surface substantially coplanar with a top surface of ~~said first portion of said first insulating layer; and with a top surface of said second portion of said first insulating layer;~~

a second insulating layer on said top surface of said die and on said top surface ~~surfaces~~ of ~~said first and second portions of said first insulating layer;~~

a patterned metal layer over said second insulating layer, ~~[[over]]~~ said top surface of said die and ~~[[over]]~~ said top surface ~~surfaces of said first and second portions of said first insulating layer, wherein said patterned metal layer comprises electroplated copper, wherein said patterned metal layer is connected to a first metal pad of said die through a first opening in said second~~

insulating layer, and wherein said patterned metal layer is connected to a second metal pad of said die through a second opening in said second insulating layer, wherein said first metal pad is connected to said second metal pad through said patterned metal layer; and

a passive device over said second insulating layer, [[; and]]

~~a metal bump directly over said top surface of said first portion of said first insulating layer, wherein said metal bump is connected to said die through said patterned metal layer.~~

180. (previously presented) The chip package in claim 179, wherein said first insulating layer comprises an epoxy.

181. (currently amended) The chip package in claim 179 further comprising multiple solder bumps configured for external connection., ~~wherein said metal bump comprises a solder.~~

182. (previously presented) The chip package in claim 179, wherein said second insulating layer comprises polyimide.

183. (previously presented) The chip package in claim 179, wherein said second insulating layer comprises benzocyclobutene (BCB).

184. (currently amended) The chip package in claim 179 further comprising a third insulating layer on said patterned metal layer[[, on]] and said passive device, and over said second insulating layer, [[over]] said top surface of said die and [[over]] said top surface ~~surfaces of said first and second portions of said first insulating layer.~~

185. (previously presented) The chip package in claim 184, wherein said third insulating layer comprises polyimide.

186. (previously presented) The chip package in claim 184, wherein said third insulating layer comprises benzocyclobutene (BCB).

187. (previously presented) The chip package in claim 179, wherein said patterned metal layer comprises a ground bus connecting said first metal pad to said second metal pad.

188. (previously presented) The chip package in claim 179, wherein said patterned metal layer comprises a power bus connecting said first metal pad to said second metal pad.

189. (previously presented) The chip package in claim 179, wherein said patterned metal layer comprises a signal trace connecting said first metal pad to said second metal pad.

190. (currently amended) The chip package in claim 179, wherein said passive device comprises further comprising a filter over said second insulating layer.

191. (previously presented) The chip package in claim 179, wherein said passive device comprises an inductor over said second insulating layer.

192. (previously presented) The chip package in claim 179, wherein said passive device comprises a capacitor over said second insulating layer.

193. (previously presented) The chip package in claim 179, wherein said passive device comprises a resistor over said second insulating layer.

194. (previously presented) The chip package in claim 179 further comprising a substrate under said die and under said first and second portions.

195. (previously presented) The chip package in claim 194, wherein said substrate comprises silicon.

196. (currently amended) The chip package in claim 179, wherein said passive device comprises a portion ~~directly~~ vertically over ~~said top surface of~~ said first portion of said first insulating layer.

197. (currently amended) A chip package comprising:

a first insulating layer;

a die between a first portion of said first insulating layer and a second portion of said first insulating layer, wherein said die has a top surface substantially coplanar with a top surface of ~~said first portion of said first insulating layer; and with a top surface of said second portion of said first insulating layer;~~

a second insulating layer on said top surface of said die and on said top surface ~~surfaces~~ of ~~said first and second portions~~ of said first insulating layer;

a patterned metal layer over said second insulating layer, ~~[[over]]~~ said top surface of said die and ~~[[over]]~~ said top surface ~~surfaces of said first and second portions~~ of said first insulating layer, ~~wherein said patterned metal layer comprises electroplated copper,~~ wherein said patterned metal layer comprises a ground piece ~~[[bus]]~~ connected to a first metal pad of said die through a first opening in said second insulating layer, and connected to a second metal pad of said die through a second opening in said second insulating layer, wherein said first metal pad is connected to said second metal pad through said ground piece; and

a passive device over said second insulating layer, ~~[[; and]]~~

~~a metal bump directly over said top surface of said first portion of said first insulating portion, wherein said metal bump is connected to said die through said patterned metal layer.~~

198. (currently amended) The chip package in claim 197, wherein said passive device comprises further comprising an inductor over said second insulating layer.

199. (currently amended) The chip package in claim 197, wherein said passive device comprises further comprising a resistor over said second insulating layer.

200. (previously presented) The chip package in claim 197, wherein said first insulating layer comprises an epoxy.

201. (currently amended) The chip package in claim 197, wherein said passive device comprises further comprising a capacitor over said second insulating layer.

202. (previously presented) The chip package in claim 197, wherein said second insulating layer comprises polyimide.

203. (currently amended) The chip package in claim 197 further comprising a third insulating layer on said patterned metal layer and on said passive device.

204. (previously presented) The chip package in claim 197, wherein said second insulating layer comprises benzocyclobutene (BCB).

205. (currently amended) The chip package in claim 197 further comprising multiple solder bumps configured for external connection, ~~wherein said metal bump comprises a solder~~.

206. (previously presented) The chip package in claim 197 further comprising a substrate under said die and under said first and second portions of said first insulating layer.

207. (previously presented) The chip package in claim 206, wherein said substrate comprises silicon.

208. (currently amended) The chip package in claim 197, wherein said passive device comprises further comprising a filter over said second insulating layer.

209. (new) The chip package in claim 197, wherein said patterned metal layer comprises electroplated copper.

210. (new) The chip package in claim 179, wherein said patterned metal layer comprises electroplated copper.